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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,919	10/27/2003	Yean-Yow Hwang	015114-066600US	5082
26059	7590	06/05/2006	EXAMINER	
TOWNSEND AND TOWNSEND AND CREW LLP/ 015114 TWO EMBARCADERO CENTER 8TH FLOOR SAN FRANCISCO, CA 94111-3834				TO, TUYEN P
ART UNIT		PAPER NUMBER		
		2825		

DATE MAILED: 06/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/694,919	HWANG ET AL.
Examiner Tuyen To	Art Unit 2825	T7

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 20 March 2006.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-20 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                    | Paper No(s)/Mail Date. _____.   |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input type="checkbox"/> Other: _____.                                   |

## DETAILED ACTION

This is a response to the amendment filed on 03/20/2006. Claims 1-20 are pending.

1. Applicants' arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Objections*

Claims 15 and 16 are objected to because of the following informalities: the recited "the first function" and "the second functions" need to be clarified. Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1- 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaviani (US Patent No. 6,480,023) and further in view of Wallace (US Patent No. 6360352) or Vemuri et al., "BDD-Based Logic Synthesis for LUT-Based FPGAs", ACM Transactions on Design Automation of Electronic systems, Vol. 7, No.4, Oct. 2002, Pages 501-525.**

**Referring to claim 1 and similarly recited claim 11,** Kaviani discloses the method/ computer program product (claim11) for mapping a user function for a programmable integrated circuit to a plurality of lookup tables, the method comprising:

decomposing the user function into a first set of decomposed functions, the user function receiving input variables (*Kaviani, Figs. 1A-2, col. 2, ll. 65 to col. 3, ll. 65*);

determining whether the first set of decomposed functions can be implemented by one of a set of lookup table configurations for the programmable integrated circuit (*Kaviani, Figs 3-5; col. 2, ll. 65 to col. 3, ll. 65; col. 11, ll. 1-63*).

However, Kaviani does not disclose if none of the set of lookup table configurations can implement the first set of decomposed functions, rotating at least two of the input variables of the user function.

Wallace discloses if none of the set of lookup table configurations can implement the first set of decomposed functions, rotating at least two of the input variables of the user function (*Wallace teaches the method includes the steps of generating fanout-free regions into quasi-canonical models (“LUT”; col.8, lines 15-19) and transforming the result into swap structures so the pin swap groups and swappable pins can be identified (Fig.4; col. 5, lines 29-37); the swappable pins can be swapped or rotated as needed for modifying the circuit layout or configuration (“lookup table configurations”)( Fig. 6-8; col. 9, lines 64+ to col. 13, line 26 ) if the designed specifications are not met (col. 1, lines 39-47; col. 7, lines 58-61; col. 14, lines 45-56). Wallace also teaches that the approach can be applied for mapping a design circuit into the LUT- based FPGAs as well (col. 8, lines 8-19; col. 14, lines 11-16)*).

Vemuri et al. disclose if none of the set of lookup table configurations can implement the first set of decomposed functions, rotating at least two of the input variables of the user function (*Vemuri et al. disclose decomposing a k-infeasible function, i.e. a function that cannot be performed/implemented by a configuration of lookup tables, into a minimum number of k-feasible subfunctions by swapping a pair of input variables (Vemuri et al., sections 2.2, 4.2, and 4.3)).*

*Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teaching of Kaviani with the teachings of Wallace or Vemuri et al. because decomposing a function that was k-infeasible by swapping inputs would provide a minimum number of k-feasible subfunctions (vemuri et al.; section 4.3), thereby optimizing circuit area and circuit delay during the layout process (Wallace, col. II. 5-11).*

**Referring to claim 2,** the method according to claim 1 further comprising:  
decomposing the user function into a second set of decomposed functions  
(*Kaviani, Figs. 1A-2, col. 2, II. 65 to col. 3, II. 65*); and

determining whether the second set of decomposed functions can be implemented by one of the set of lookup table configurations for the programmable integrated circuit (*Kaviani, Figs 3-5; col. 2, II. 65 to col. 3, II. 65; col. 11, II. 1-63*).

**Referring to claim 3 and similarly recited claim 12,** the method according to claim 1 and claim 11 respectively, further comprising:

if the user function is not successfully decomposed into a set of decomposed

functions (*Vemuri et al.*, sections 2.2 and 4.3), rotating at least two of the input variables of the user function (*Vemuri et al.*, sections 2.2 and 4.3); and attempting to decompose the user function into a second set of decomposed functions (*Vemuri et al.*, sections 2.2 and 4.1-4.3).

**Referring to claim 4 and similarly recited claim 17,** the method according to claims 1 and 11, respectively, further comprising:

if one of the lookup table configurations can implement the first set of decomposed functions, placing lookup tables in the lookup table configuration into logic blocks on the programmable integrated circuit (*Kaviani*, Fig. 4A, col. 11, ll. 1-43); and configuring programmable routing resources to connect the logic blocks on the programmable integrated circuit (*Kaviani*, Fig. 4A, col. 11, ll. 1-43; Fig. 7B, col. 14, ll. 3-25).

**Referring to claim 5, 7, 18-19:**

(Claim 5 and similarly recited claim 18)

The method according to claim 4 and claim 11 respectively, wherein one of the lookup table configurations includes two 5-input lookup tables and one 6-input lookup table.

(Claim 7 and similarly recited claim 19)

The method according to claim 4 and claim 11 respectively, wherein one of the lookup table configurations includes two 4-input lookup tables and one 6-input lookup table.

*Wallace reference suggests that in Fig. 7-8, each decomposition function block (AND, OR, MUX) in the block configurations may have two or more input variables (col. 5, lines 21-28).*

*It would have been obvious one of ordinary skill in the art at the time of the invention to design primitive gates to have two 5-input (or two 4-input) lookup tables and one 6-input lookup table because this reduce number of lookup tables and logic blocks implemented within the programmable IC as required by design specification.*

**Referring to claim 6,** the method according to claim 4 wherein at least two of the input variables are shared between two of the lookup tables (*Kaviani, col. 6ll. 65 to col. 7, ll. 14; Fig. 4A, col. 11, ll. 1-43*).

**Referring to claim 8 and similarly recited claim 13,** the method according to claims 1 and 11, respectively, wherein decomposing the user function into the first set of decomposed functions further comprises decomposing the user function into first stage functions and a second stage function (*Kaviani, Fig. 4A, col. 111, ll. 1-43*), outputs of the first stage functions being inputs into the second stage function (*Kaviani, Fig. 4A, col. 111, ll. 1-43*).

**Referring to claim 9,** the method according to claim 8 wherein rotating at least two of the input variables of the user function further comprises swapping at least one of the input variables of the first stage functions with at least one of the input variables of the second stage function (*Wallace, Figs. 2 and 7-8; col. 3, ll. 19-30, col. 11, ll. 47 to col. 14, ll. 32*).

**Referring to claim 10,** the method according to claim 9 further comprising:

attempting to decompose the user function into a second set of decomposed functions based on the rotated-input variables (*Vemuri et al., sections 2.2 and 4.1-4.3*).

**Referring to claim 14**, the computer program product according to claim 13 wherein the code (*Wallace, col. 15, lines 36-49*) for decomposing further comprises:

code for decomposing the user function into a second set of decomposed functions based on the rotated input variables (*Wallace, col. 15, lines 36-49*), the second set of decomposed functions including first stage functions and a second stage function (*Wallace ,Fig. 6-8; col. 13, lines 21-26*),

wherein at least two input variables of the first and the second stages of the a set of decomposed functions have been rotated with respect to input variables of the first and the second stages of the first set of decomposed functions (*Wallace , Fig. 7-8; col. 15, lines 36-49*).

**Referring to claim 15**, the computer program product according to claim 11 wherein the code for decomposing the first function into the second functions further comprises code for decomposing the first function into the second functions using a non-disjoint decomposition technique (*Vemuri et al., section 4.2*).

**Referring to claim 16**, the computer program product according to claim 11 wherein the code for decomposing the first function into the second functions further comprises code for decomposing the first function into the second functions using a disjoint decomposition technique (*Wallace, col. 15, lines 36-49; col. 4, lines 53+; col. 5, lines 1-28*).

**Referring to claim 20,** the computer program product according to claim 11 further comprising:

code for decomposing the user function into a second set of decomposed functions based on the rotated input variables, if none of the configurations of lookup tables can implement the first set of decomposed functions (*Vemuri et al. disclose decomposing a k-infeasible function, i.e. a function that cannot be performed/implemented by a configuration of lookup tables, into a minimum number of k-feasible subfunctions by swapping a pair of input variables* (*Vemuri et al., sections 2.2, 4.2, and 4.3*) ); and

code for determining whether the second set of decomposed functions can be implemented by one of the configurations of lookup tables for the programmable integrated circuit (*Kaviani, Figs 3-5; col. 2, ll. 65 to col. 3, ll. 65; col. 11, ll. 1-63*).

### ***Conclusion***

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272- 7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Art Unit: 2825

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Tuyen To

Patent Examiner

AU 2825

  
JACK CHIANG  
SUPERVISORY PATENT EXAMINER